Assignee: Intel Corporation

CLAIMS

What is claimed is:

1   1.   A processor, comprising:

2   a first register alias table including a first number of read ports to

3   translate a first set of logical register addresses to physical register

4   addresses; and

5   a second register alias table including a second number of read

6   ports to translate a second set of logical register addresses to physical

7   register addresses, wherein said first number is greater than said

8   second number.

1   2.   The processor of claim 1, wherein said first number is

2   proportional to a third number of logical register addresses in said first

3   set.

1   3.   The processor of claim 1, further comprising pipeline logic

2   to stall a pipeline when a first instruction utilizes more logical register

3   addresses from said second set than said second number.

1   4.   The processor of claim 1, further comprising a trace cache

2   to supply a trace of micro-operations to said first register alias table and

3   said second register alias table.

1   5.   The processor of claim 4, wherein said trace cache includes

2   trace cache logic to build said trace limiting a third number of live-in

3   and live-out logical registers to said second number.

1   6.   A method, comprising:

2   storing frequently used translations from logical register

3   addresses to physical register addresses in a first register alias table;

4   and

5   storing less-frequently used translations from logical register

6   addresses to physical register addresses in a second register alias table,

7   where said second register alias table has fewer read ports than said

8   first register alias table.

1   7.   The method of claim 6, wherein said storing less-frequently

2   used translations includes identifying said less-frequently used

3   translations from a set of logical register addresses.

1   8.   The method of claim 7, wherein said identifying includes

2   selecting infrequently used temporary registers.

1   9.   The method of claim 8, wherein said infrequently used

2   temporary registers are associated with a long micro-operation flow.

1   10.   The method of claim 7, wherein said identifying includes

2   selecting control registers.

1   11.   The method of claim 10, wherein said identifying includes

2   choosing registers used by a compiler.

1   12.   The method of claim 6, further comprising building a trace

2   in a trace cache whose micro-operations require no more live-in

3   registers and live-out registers using said second register alias table

4   than a first number of read ports of said second register alias table.

1   13.   The method of claim 12, wherein said building includes

2   permitting no more live-out registers using said second register alias

3   table than a second number of write ports of said second register alias

4   table.

1   14.   The method of claim 6, further comprising stalling a

2   pipeline when a first number of logical register addresses is supplied to

3   said second register alias table, and said first number is greater than a

4   second number of read ports of said second register alias table.

1   15.   An apparatus, comprising:

2   means for storing frequently used translations from logical

3   register addresses to physical register addresses in a first register alias

4   table; and

5   means for storing less-frequently used translations from logical

6   register addresses to physical register addresses in a second register

7   alias table, where said second register alias table has fewer read ports

8   than said first register alias table.

1   16.   The apparatus of claim 15, wherein said means for storing

2   less-frequently used translations includes means for identifying said

3   less-frequently used translations from a set of logical register addresses.

1   17.   The apparatus of claim 15, further comprising means for

2   building a trace in a trace cache whose micro-operations require no

3   more live-in registers and live-out registers using said second register

4   alias table than a first number of read ports of said second register alias

5   table.

1   18.   The apparatus of claim 17, wherein said means for building

2   includes means for permitting no more live-out registers using said

3   second register alias table than a second number of write ports of said

4   second register alias table.

1   19.   The apparatus of claim 15, further comprising means for

2   stalling a pipeline when a first number of logical register addresses is

3   supplied to said second register alias table, and said first number is

4   greater than a second number of read ports of said second register alias

5   table.

1   20.   A system, comprising:

2   a processor including a first register alias table including a first

3   number of read ports to translate a first set of logical register addresses

4   to physical register addresses, and a second register alias table

5   including a second number of read ports to translate a second set of

6   logical register addresses to physical register addresses, wherein said

7   first number is greater than said second number;

8   an audio input/output device; and

9   an interface to couple said processor to said audio input/output

10 device.

1   21.   The system of claim 20, wherein said first number is

2   proportional to a third number of logical register addresses in said first

3   set.

1   22.   The system of claim 20, further comprising pipeline logic to

2   stall a pipeline when a first instruction utilizes more logical register

3   addresses from said second set than said second number.

1   23.   The system of claim 20, further comprising a trace cache to

2   supply a trace of micro-operations to said first register alias table and

3   said second register alias table.

1   24.   The system of claim 23, wherein said trace cache includes

2   trace cache logic to build said trace limiting a third number of live-in

3   and live-out logical registers to said second number.